# QFN Evaluation

## TMV/TSV Status

by

**Reza Ghaffarian, Ph.D.**

*NASA-JPL-CalTech*

**(818) 354-2059**

**Reza.Ghaffarian@JPL.NASA.gov**

Jet Propulsion Laboratory
National Aeronautics & Space Administration
California Institute of Technology

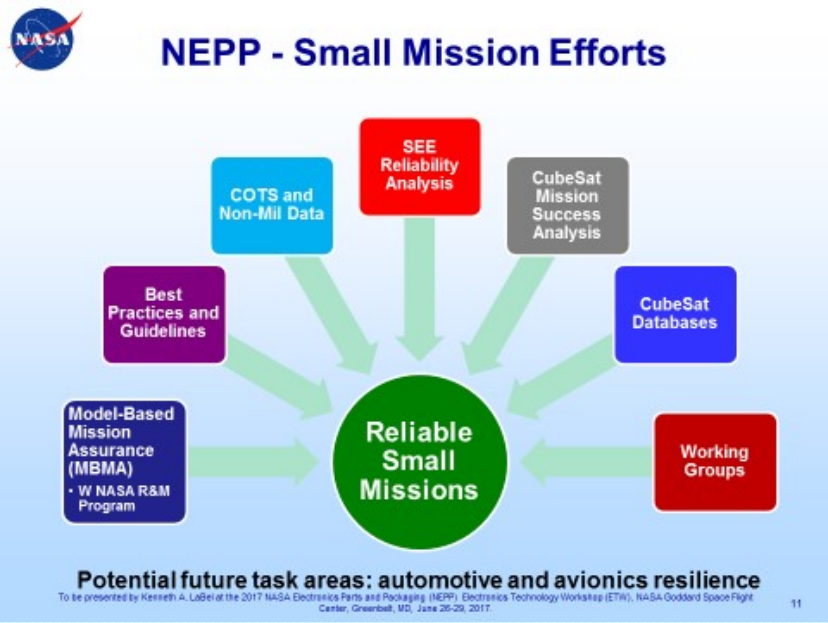


**NEPP Electronics Technology Workshop (ETW 2017)**
**June 26-29,2017, NASA GSFC**

**http://nepp.nasa.gov**

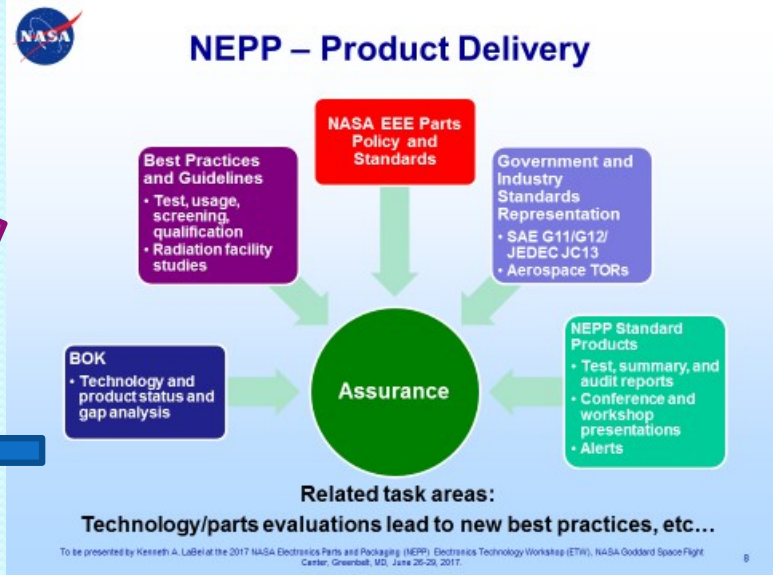
# QFN TC Reliability

**BOK**
**Guideline**
**Test Results**
**NEPP**
**Website**




**Best Practices and Guidelines**

- Test, usage, screening, qualification
- Radiation facility studies




**BOK**

- Technology and product status and gap analysis

# Outline

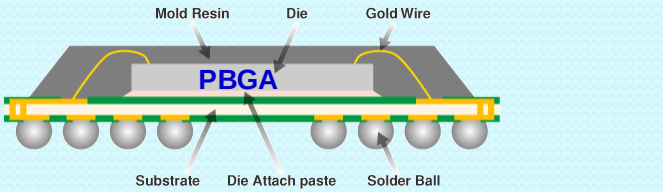
- Single Packaging Trends
  - QFN use projections
- QFN Packages/Assemblies
  - Various sizes and I/Os
  - Tin-lead and Pb-free on ENIG PCB finish
  - X-ray/Optical evaluation
- Thermal Shock Cycles (TSC)
  - 200 TSC1 (-55°C/100°C)
  - > 1000 TSC2 (-55°C/125°C)
  - Age at 125°C for 250 hour plus TSC2
  - Failure analyses by X-section
- Summary

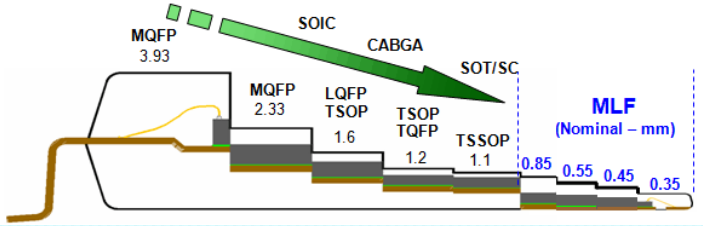
# Single Chip Packaging

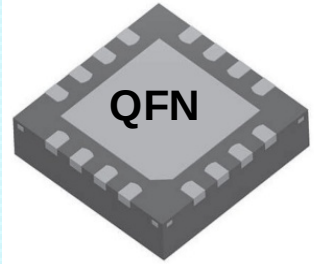
PBGA/SOC
QFN/MLF

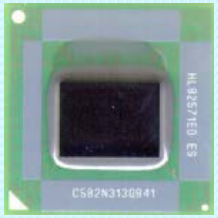
*Wire bond to Flip Chip*
*CBGA to CCGA*

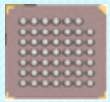
CSP / WLP
a/M/W-
QFN/LGA



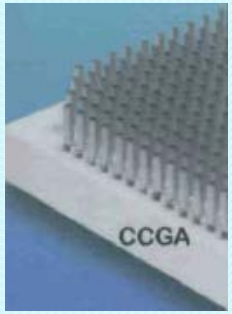



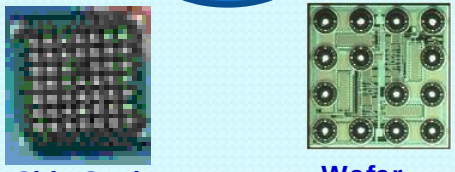





CBGA


2116 FCBGA
ASIC

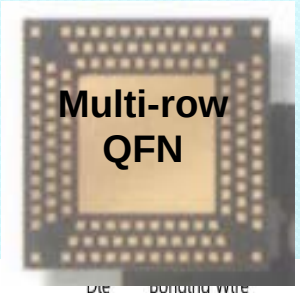


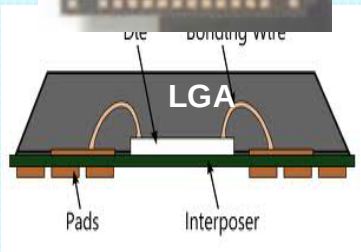



Chip Scale
Packaging
(CSP)



Wafer
Level
Packaging






*Reza Ghaffarian/JPL/Caltech*

# OFN CAAGR to 2026

| Package Style (Bn Units) | 2010 | 2011 | 2016 | CAAGR 2016/2011 | % of IC 2016 |
|---|---|---|---|---|---|
| DIP/SOT | 5.3 | 4.3 | 3.9 | -1.9% | 1.4% |
| SO/TSOP/SOT | 83.0 | 80.8 | 108.4 | 6.0% | 37.8% |
| QFP/LCC | 19.0 | 18.3 | 24.5 | 6.0% | 8.6% |
| QFN | 19.6 | 20.5 | 46.0 | 17.0% | 16.1% |

| (Bn Units) | 2015 | 2020F | 2025F | CAAGR 2015 – 2020 | CAAGR 2020 – 2025 |
|---|---|---|---|---|---|
| DIP/SOT | 3.3 | 3 | 2.6 | -1.9% | -2.8% |
| SO/TSOP/SOT | 78 | 79 | 75 | 0.3% | -1.0% |
| QFP/LCC | 14.3 | 13 | 11 | -1.9% | -3.3% |
| QFN | 37.2 | 58 | 74 | 9.3% | 5.0% |
| Wire Bond CSP | 9.9 | 12 | 14 | 3.9% | 3.7% |
| Stacked CSP | 8.7 | 11 | 12 | 4.8% | 1.8% |
| BOC | [illegible] | 6.2 | [illegible] | -2.7% | [illegible] |
| Wire Bond BGA | 0.[illegible] | 0.7[illegible] | [illegible] | -2.6% | [illegible] |
| COB (Wire Bond) | [illegible] | 15 | 16 | [illegible].9% | [illegible].3% |
| Wire Bond SiP | [illegible] | 3.1 | [illegible] | -4.5% | -0.7% |
| Flip Chip SiP | 1.1 | 4.9 | 9 | 35% | 13% |
| Flip Chip CSP | 3.6 | 4.8 | 8.5 | 5.9% | 12% |
| Flip Chip CSP for DRAM | 2.8 | 5.5 | 8 | 14% | 7.8% |
| Flip Chip QFN/MIS | 0.8 | 4 | 12 | 38% | 25% |
| Flip Chip BGA/PGA/LGA | 0.9 | 0.9 | 0.9 | 0.0% | 0.0% |
| DCA Flip Chip | 6 | 7.8 | 9 | 5.4% | 2.9% |
| Fan-in WLCSP | 20.8 | 33 | 40 | 9.7% | 3.9% |
| Fan-Out WLCSP | 0.2 | 2 | 10 | 58% | 38% |
| COG | 4.1 | 4.6 | 5.4 | 2.3% | 3.3% |
| COF | 3.5 | 4.5 | 5 | 5.2% | 2.1% |
| Subtotal Wire Bond | 176.2 | 201 | 212.2 | 2.7% | 1.1% |
| Subtotal Flip Chip | 43.8 | 72 | 107.8 | 10.5% | 8.4% |
| **IC TOTAL** | **220** | **273** | **320** | **4.4%** | **3.2%** |

**QFN 9.3% & 5.0%**

Source iNEMI 2015 & 2017

# OFN CAAGR to 2026

| Package Style (Bn Units) | 2010 | 2011 | 2016 | CAAGR 2016/2011 | % of IC 2016 |
|---|---|---|---|---|---|
| DIP/SOT | 5.3 | 4.3 | 3.9 | -1.9% | 1.4% |
| SO/TSOP/SOT | 83.0 | 80.8 | 108.4 | 6.0% | 37.8% |
| QFP/LCC | 19.0 | 18.3 | 24.5 | 6.0% | 8.6% |
| QFN | 19.6 | 20.5 | 46.0 | 17.0% | 16.1% |

| (Bn Units) | 2015 | 2020F | 2025F | CAAGR 2015 – 2020 | CAAGR 2020 – 2025 |
|---|---|---|---|---|---|
| DIP/SOT | 3.3 | 3 | 2.6 | -1.9% | -2.8% |
| SO/TSOP/SOT | 78 | 79 | 75 | 0.3% | -1.0% |
| QFP/LCC | 14.3 | 13 | 11 | -1.9% | -3.3% |
| QFN | 37.2 | 58 | 74 | 9.3% | 5.0% |
| Wire Bond CSP | 9.9 | 12 | 14 | 3.9% | 3.7% |
| Stacked CSP | 8.7 | 11 | 12 | 4.8% | 1.8% |
| BOC | [illegible] | 6.2 | [illegible] | -2.7% | [illegible] |
| Wire Bond BGA | 0.[illegible] | 0.7[illegible] | [illegible] | -2.6% | [illegible] |
| COB (Wire Bond) | [illegible] | 15 | 16 | [illegible].9% | [illegible].3% |
| Wire Bond SiP | [illegible] | 3.1 | [illegible] | -4.5% | -0.7% |
| Flip Chip SiP | 1.1 | 4.9 | 9 | 35% | 13% |
| Flip Chip CSP | 3.6 | 4.8 | 8.5 | 5.9% | 12% |
| Flip Chip CSP for DRAM | 2.8 | 5.5 | 8 | 14% | 7.8% |
| Flip Chip QFN/MIS | 0.8 | 4 | 12 | 38% | 25% |
| Flip Chip BGA/PGA/LGA | 0.9 | 0.9 | 0.9 | 0.0% | 0.0% |
| DCA Flip Chip | 6 | 7.8 | 9 | 5.4% | 2.9% |
| Fan-in WLCSP | 20.8 | 33 | 40 | 9.7% | 3.9% |
| Fan-Out WLCSP | 0.2 | 2 | 10 | 58% | 38% |
| COG | 4.1 | 4.6 | 5.4 | 2.3% | 3.3% |
| COF | 3.5 | 4.5 | 5 | 5.2% | 2.1% |
| Subtotal Wire Bond | 176.2 | 201 | 212.2 | 2.7% | 1.1% |
| Subtotal Flip Chip | 43.8 | 72 | 107.8 | 10.5% | 8.4% |
| **IC TOTAL** | **220** | **273** | **320** | **4.4%** | **3.2%** |

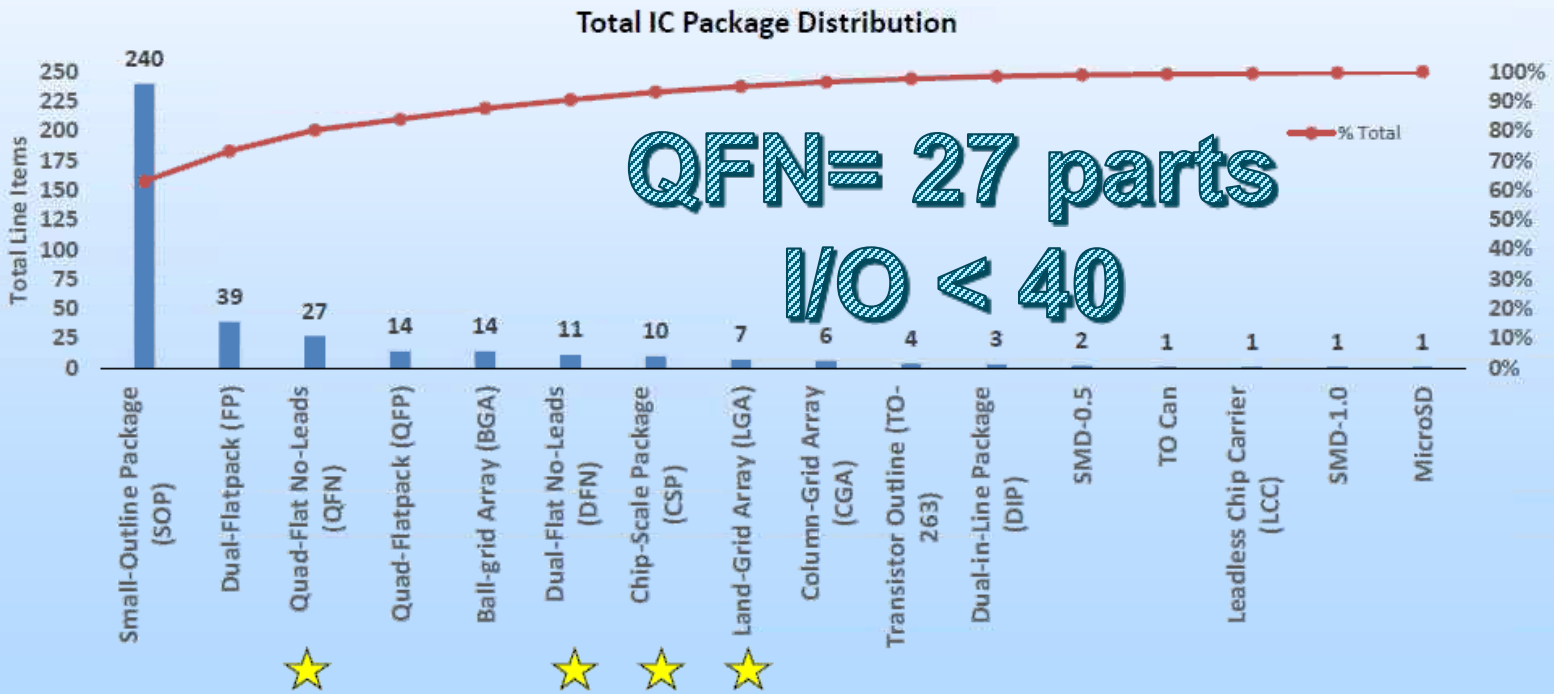
**QFN 9.3% & 5.0%**

Source iNEMI 2015 & 2017

# QFN CubeSat

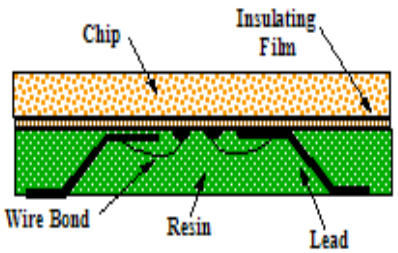
## Digging Into the Data – Actives (1 of 3)

- Small-Outline Package (SOP) and Dual-Flatpacks (FP) account for ~75% of IC packages
  - ★ Future research focus on QFN/DFNs, CSPs and LGAs may be beneficial

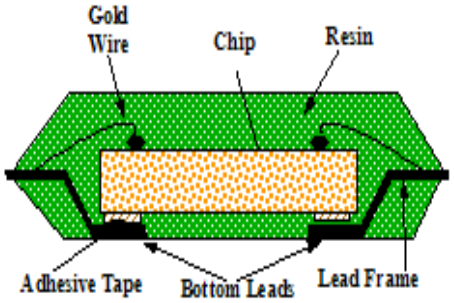



*Ref: M. Sundgaard, ETW2016*

# QFN Trends

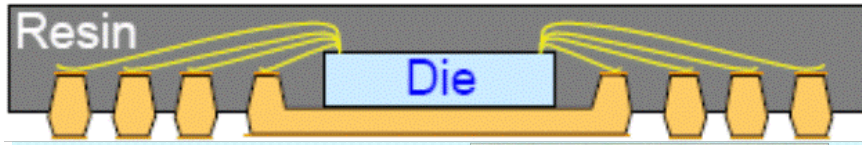


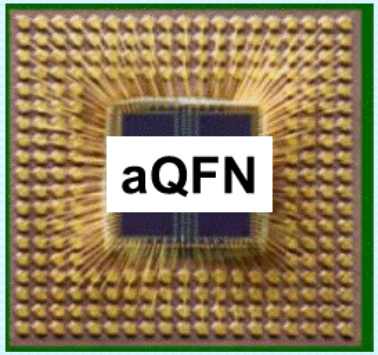

Lead On Chip
LOC

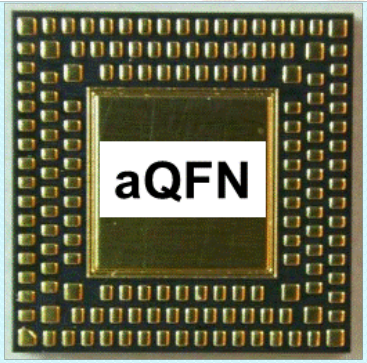



Ultra-Thin-Small-Outline
USON

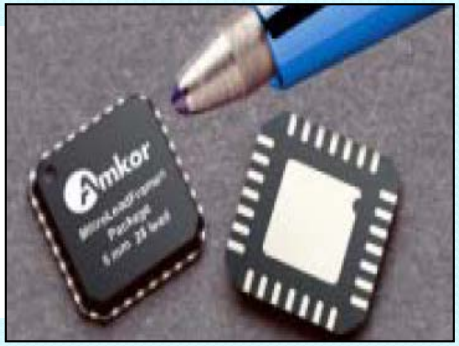
## Emerging

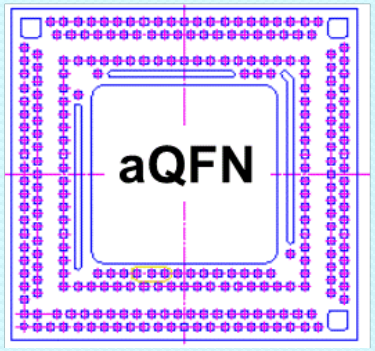


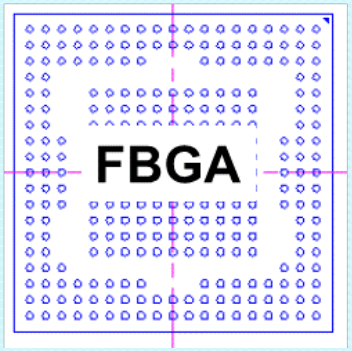




MicroLead Frame®



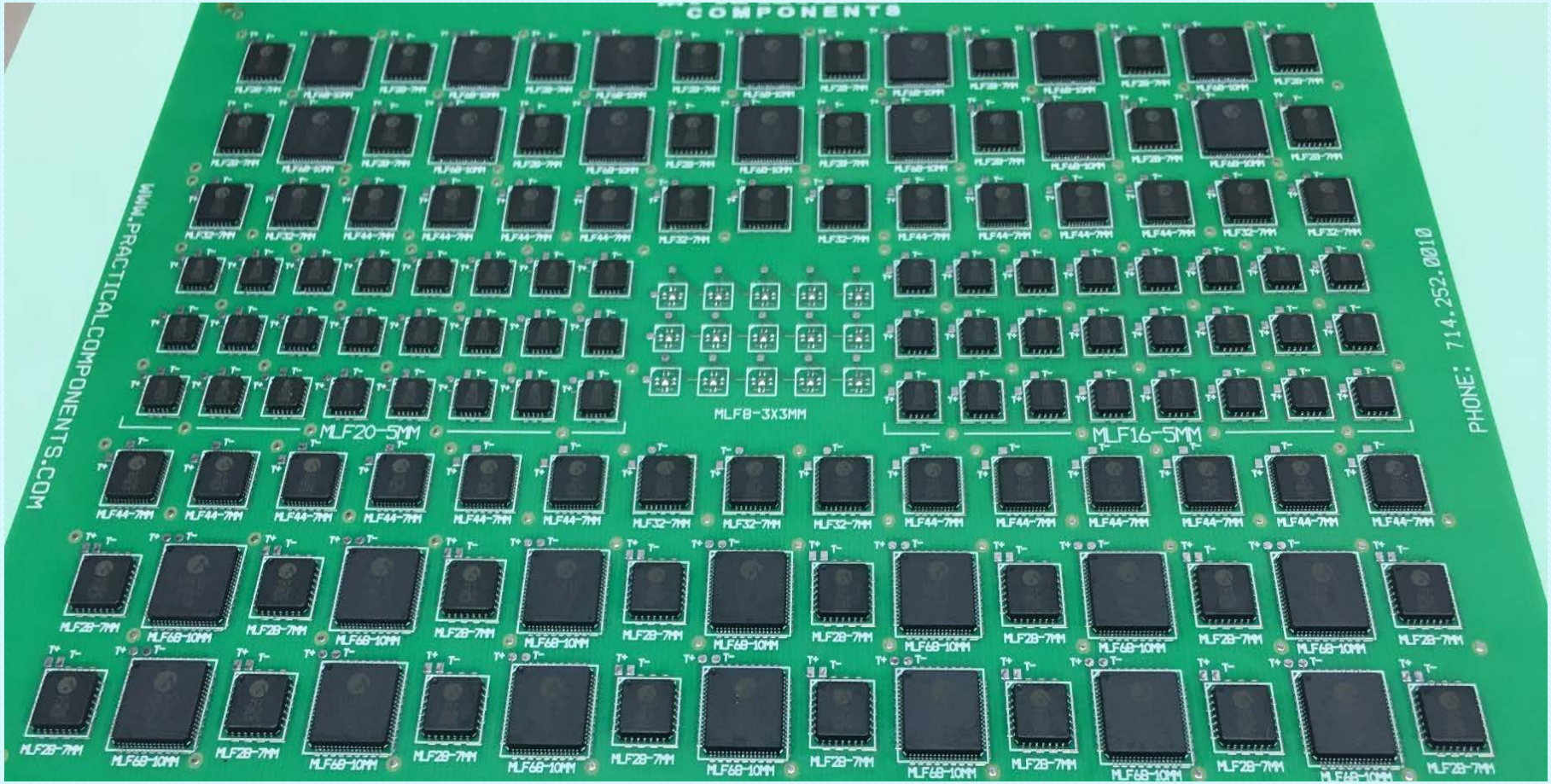




## Standard

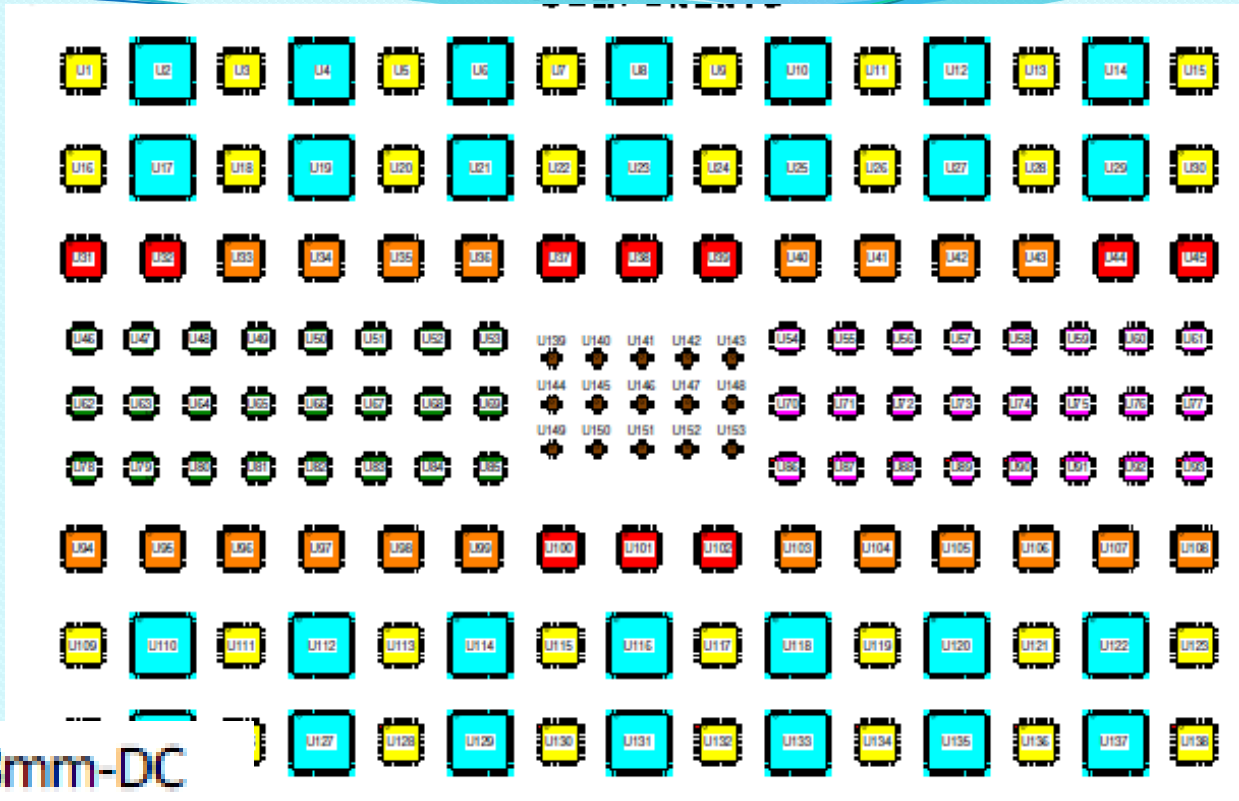


***Reza Ghaffarian/JPL/Caltech***

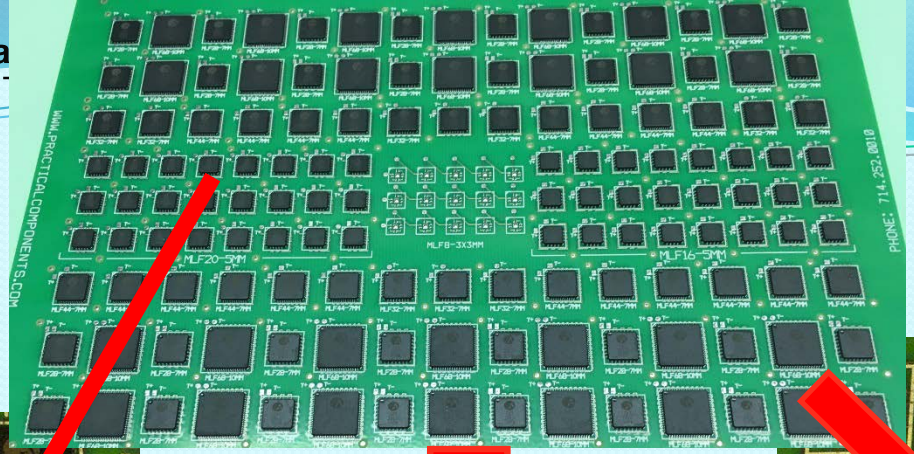
# QFN Assemblies

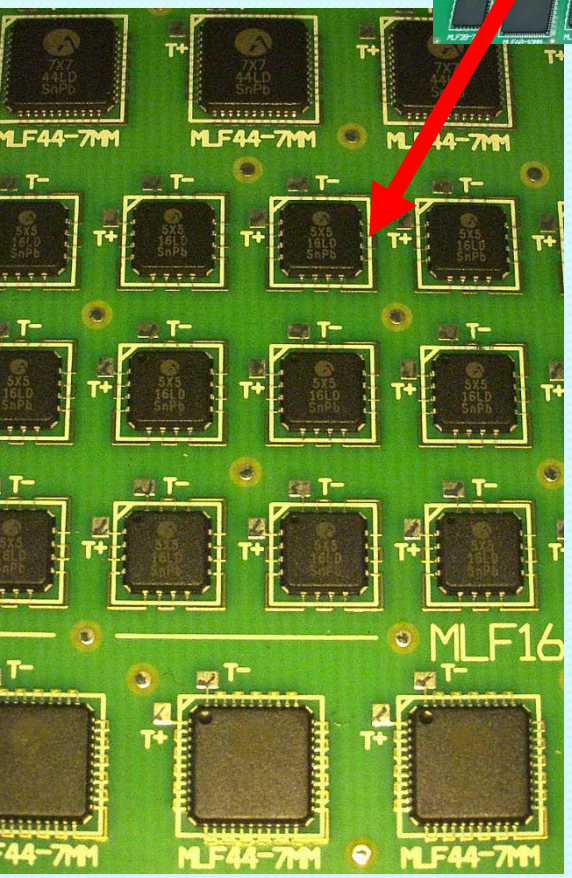


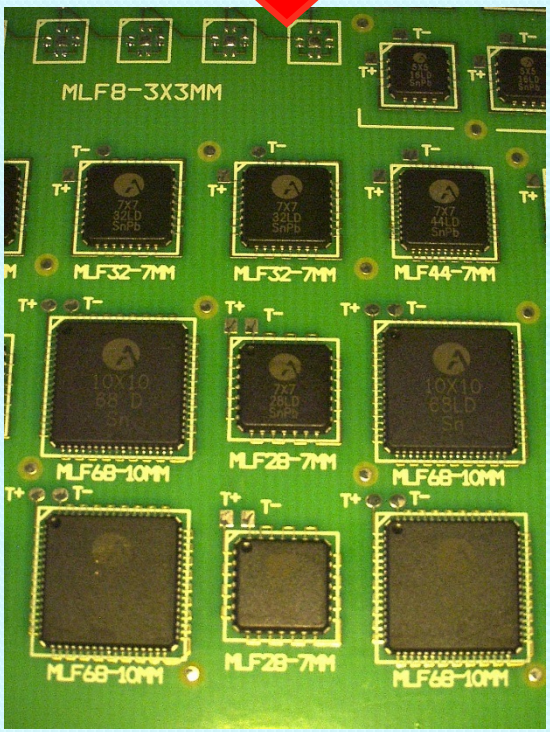
# QFN Types



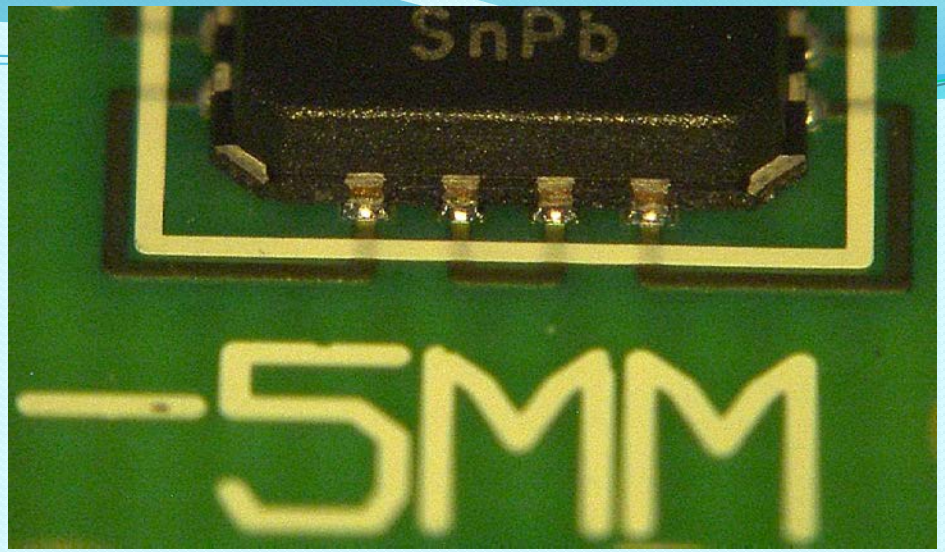
| | |
|---|---|
| | A-MLF28-7mm-.8mm-DC |
| | A-MLF68-10mm-.5mm-DC |
| | A-MLF32-7mm-.65mm-DC |
| | A-MLF44-7mm-.5mm-DC |
| | A-MLF20-5mm-.65mm-DC |
| | A-MLF16-5mm-.8mm-DC |

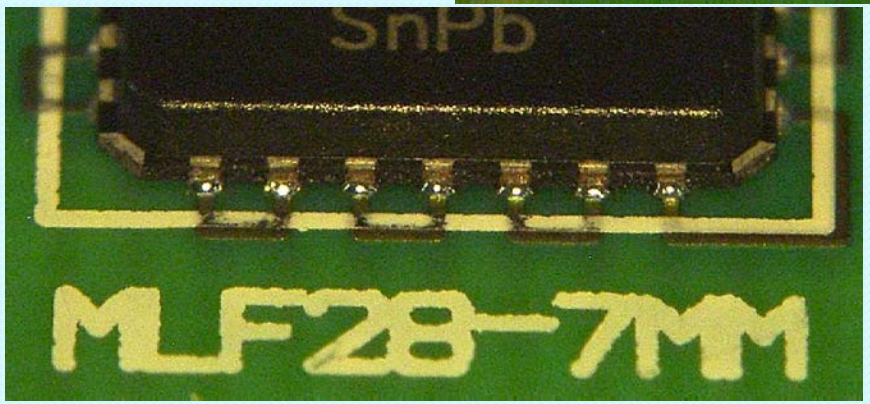

MLF20-5MM
MLF8-3X3MM
MLF16-5MM

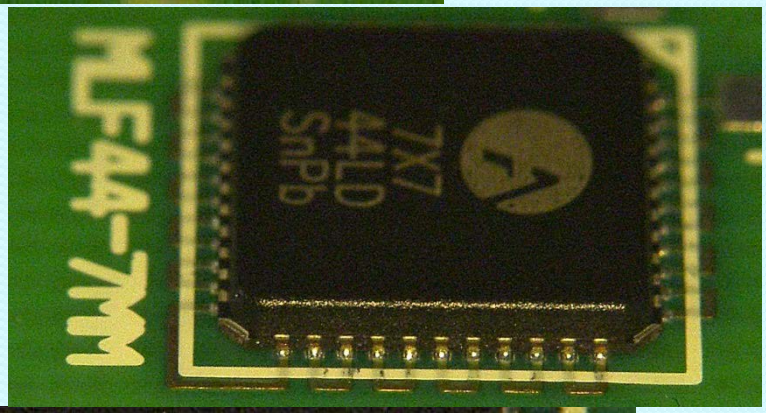

MLF44-7MM
MLF44-7MM
MLF16
MLF44-7MM
MLF44-7MM

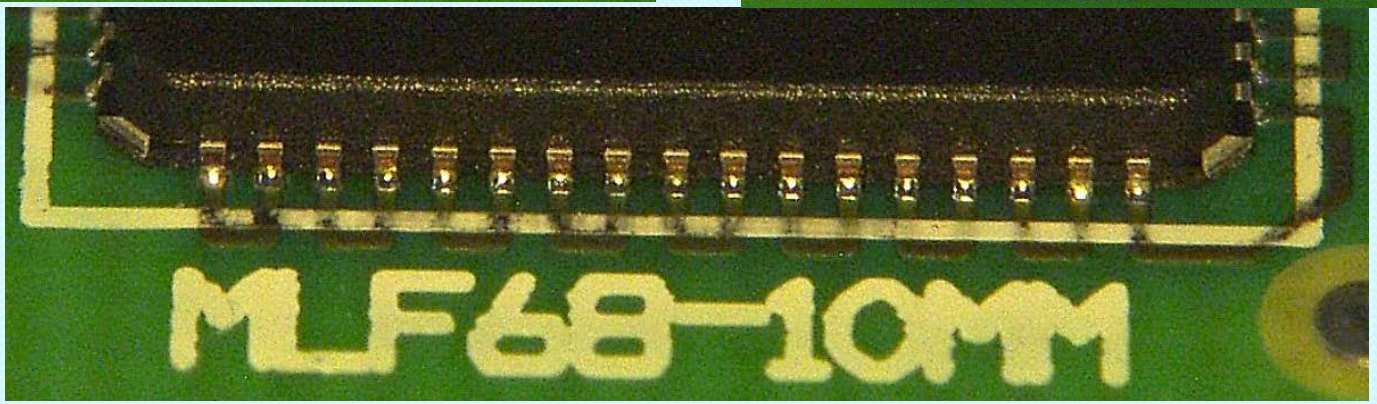

MLF8-3X3MM
MLF32-7MM
MLF32-7MM
MLF44-7MM
MLF68-10MM
MLF28-7MM
MLF68-10MM
MLF68-10MM
MLF28-7MM
MLF68-10MM


MLF16-5MM
MLF44-7MM
MLF44-7MM
MLF44-7MM
MLF28-7MM
MLF68-10MM
MLF28-7MM
MLF28-7MM
MLF68-10MM
MLF28-7MM



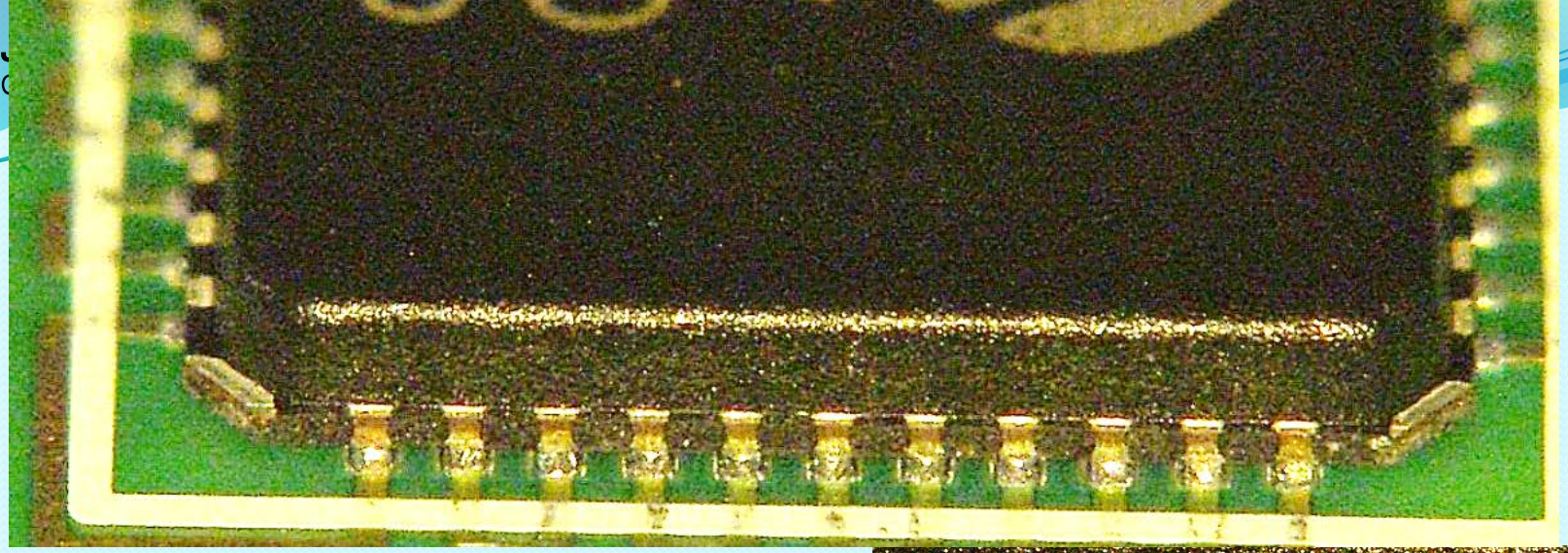



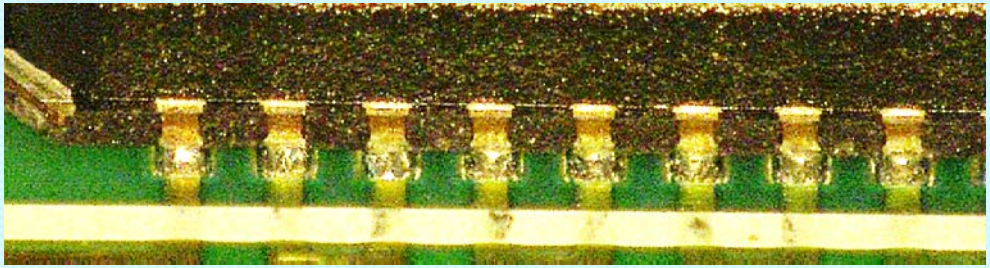



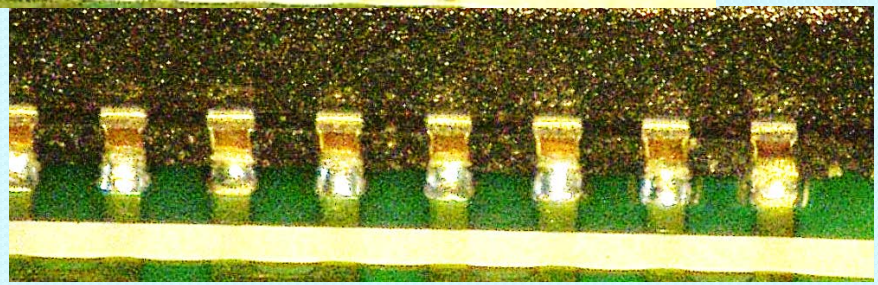



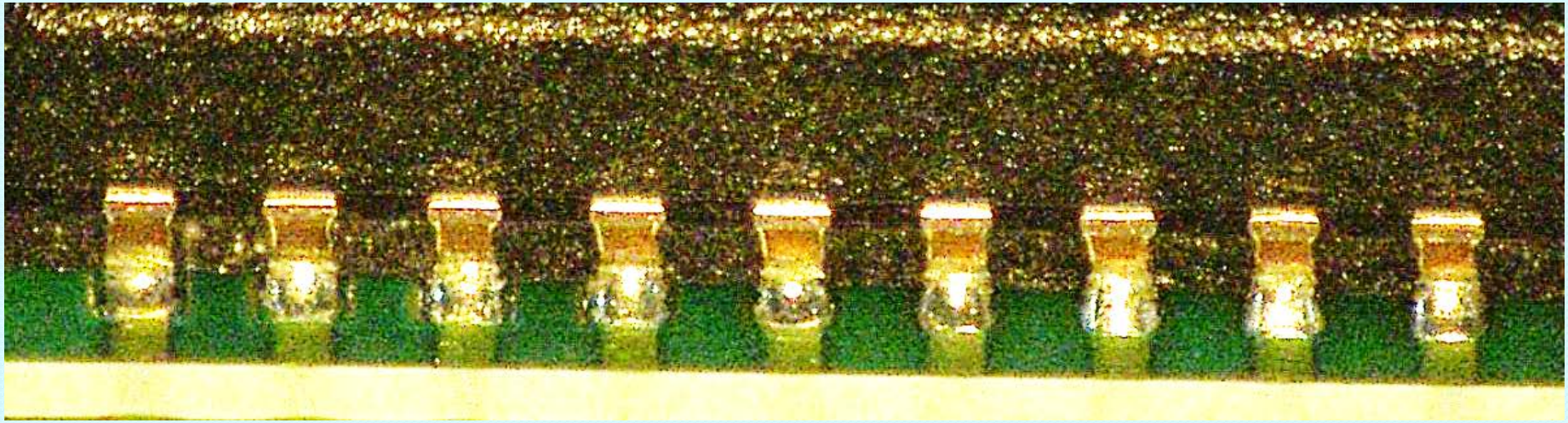


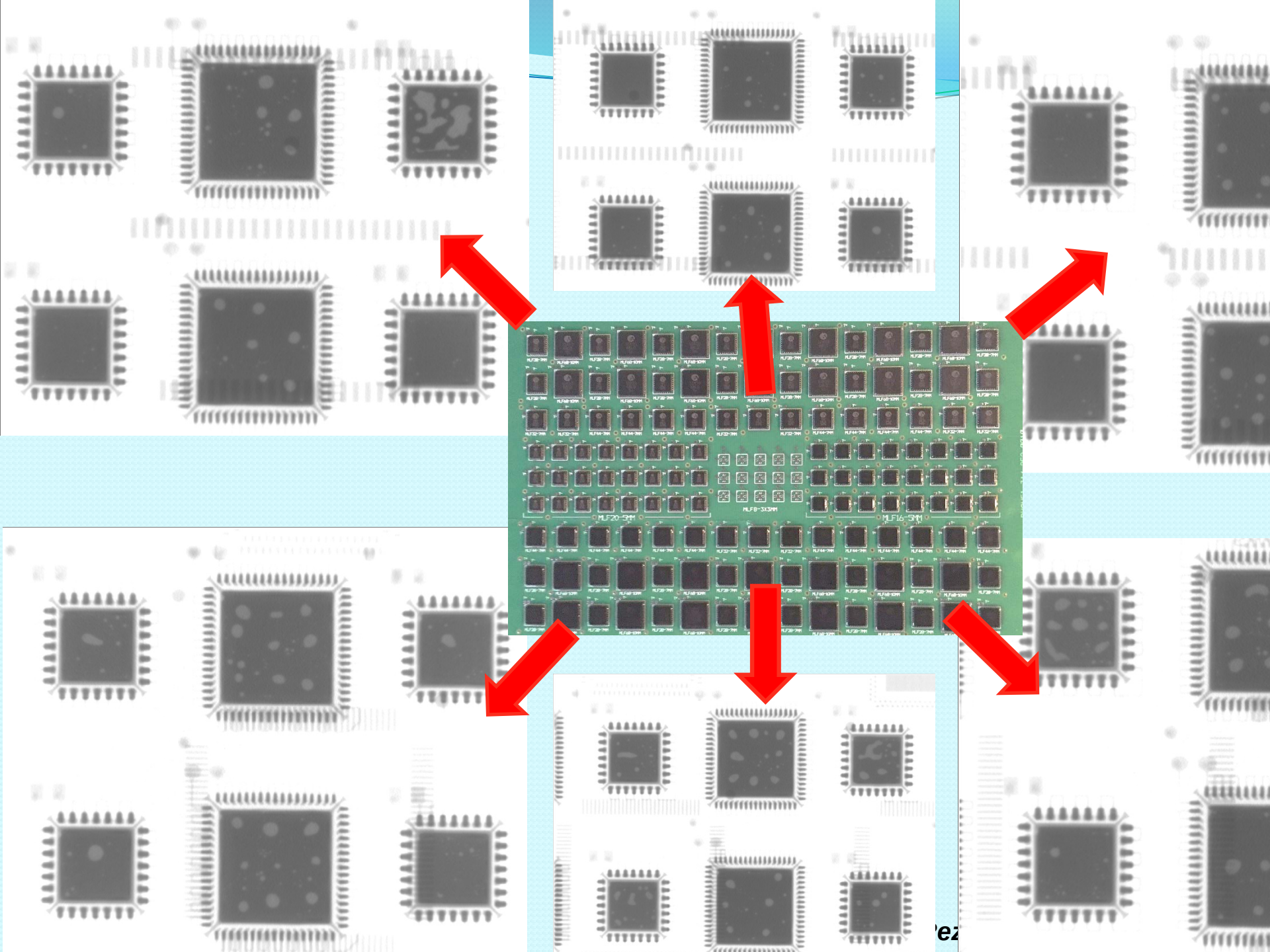

***Reza Ghaffarian/JPL/Caltech***



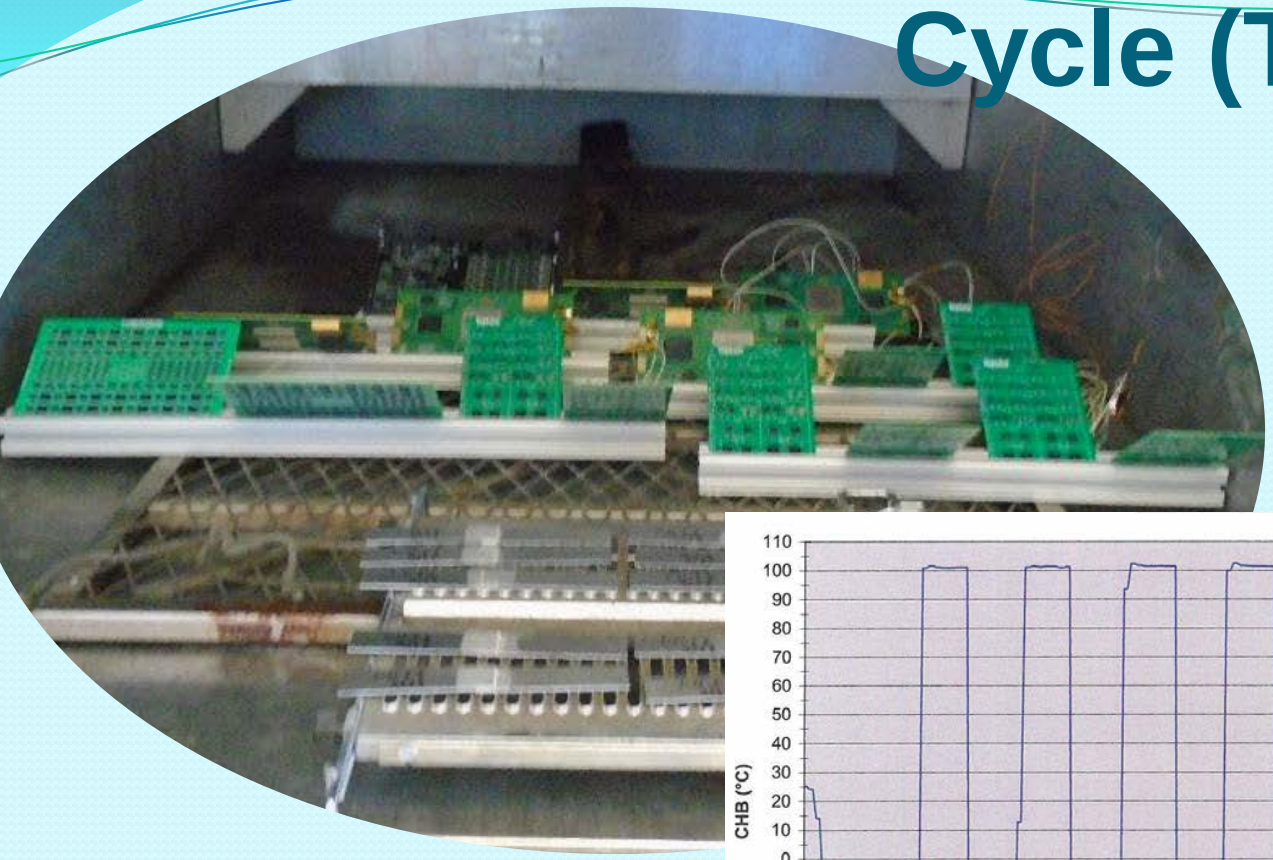




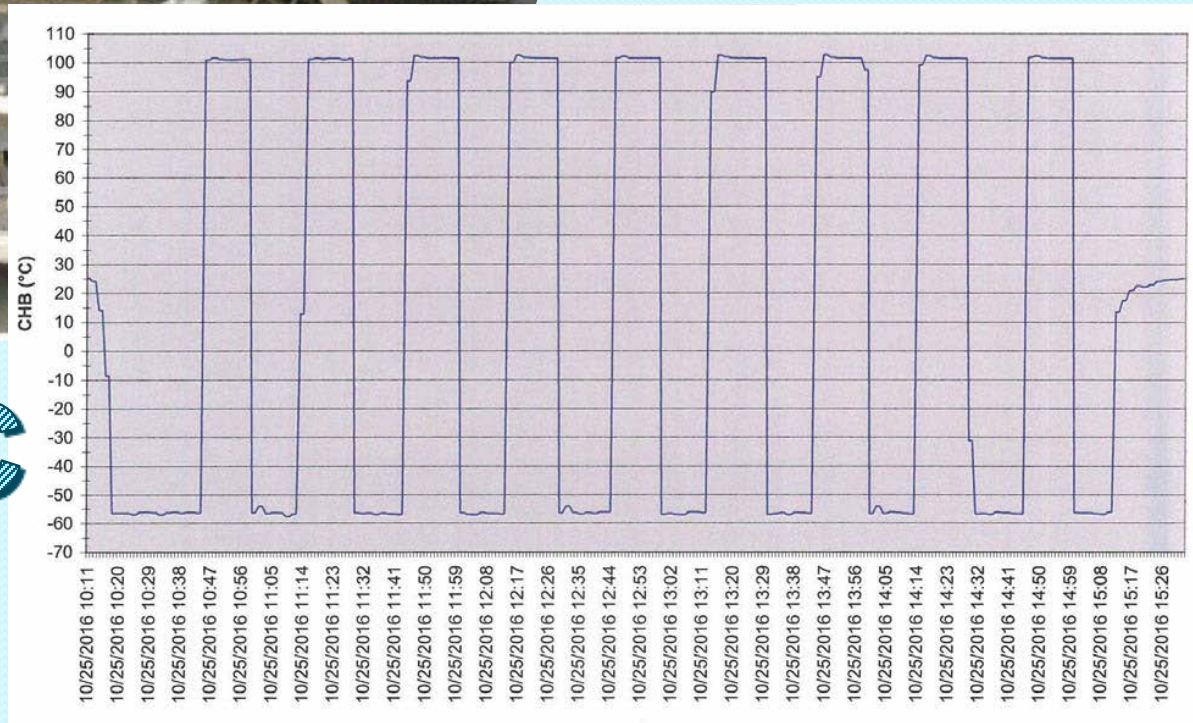



MLF20-5MM
MLF8-3X3MM
MLF16-5MM

# QFNs-Thermal Shock Cycle (TSC1)



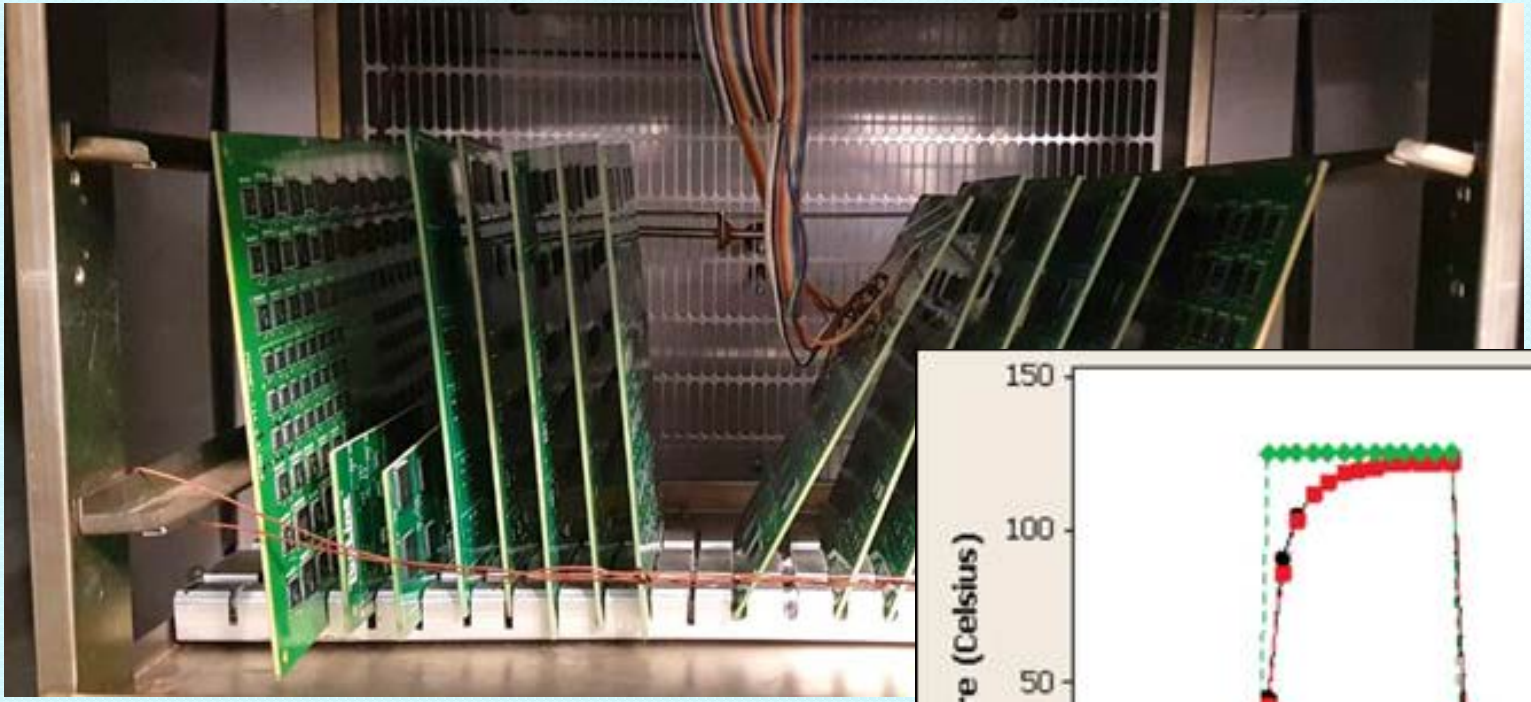
**-55°C/100°C**

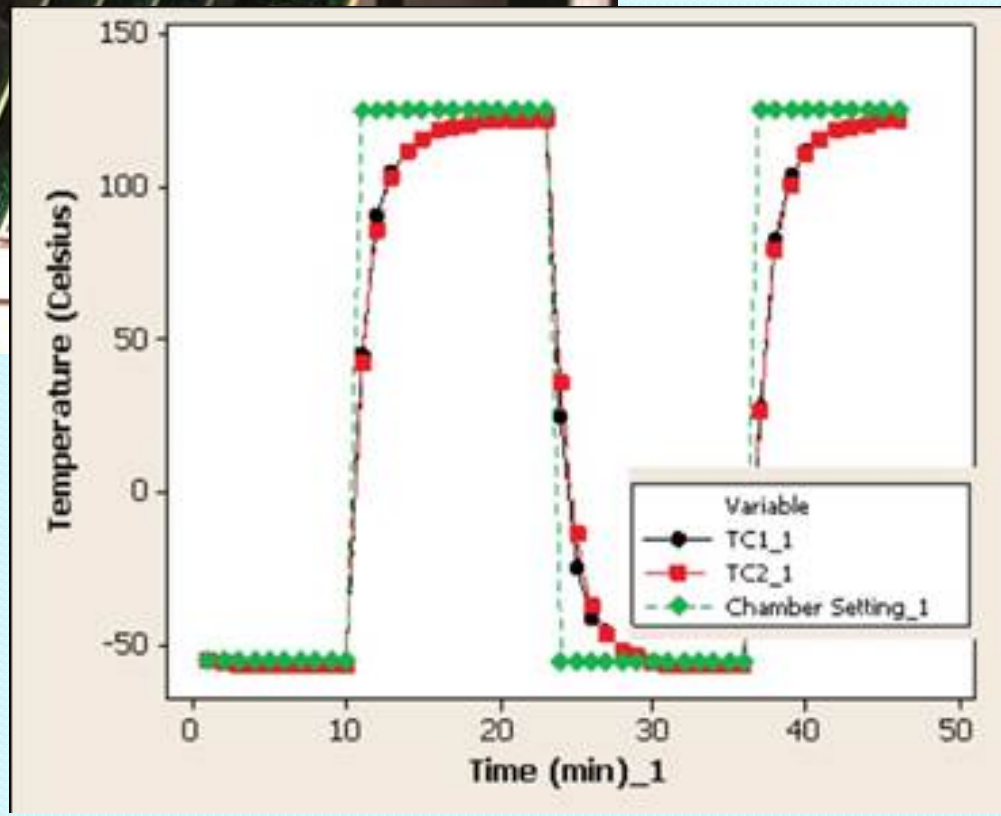





***Reza Ghaffarian/JPL/Caltech***

# QFNs-TSC2



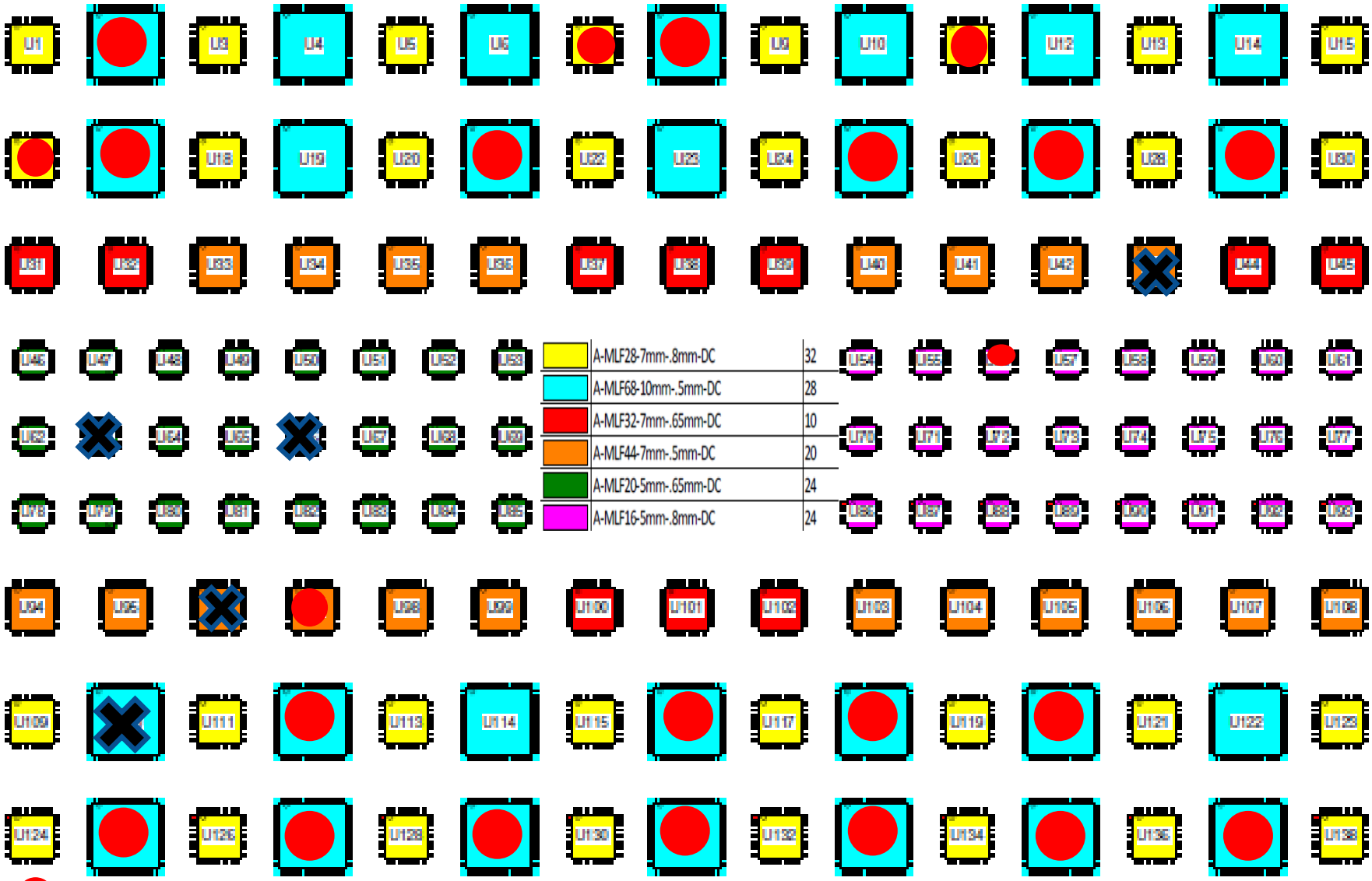



## -55°C/125°C



***Reza Ghaffarian/JPL/Caltech***

# QFN Failure 1116 TSC2 SnPb No Aging



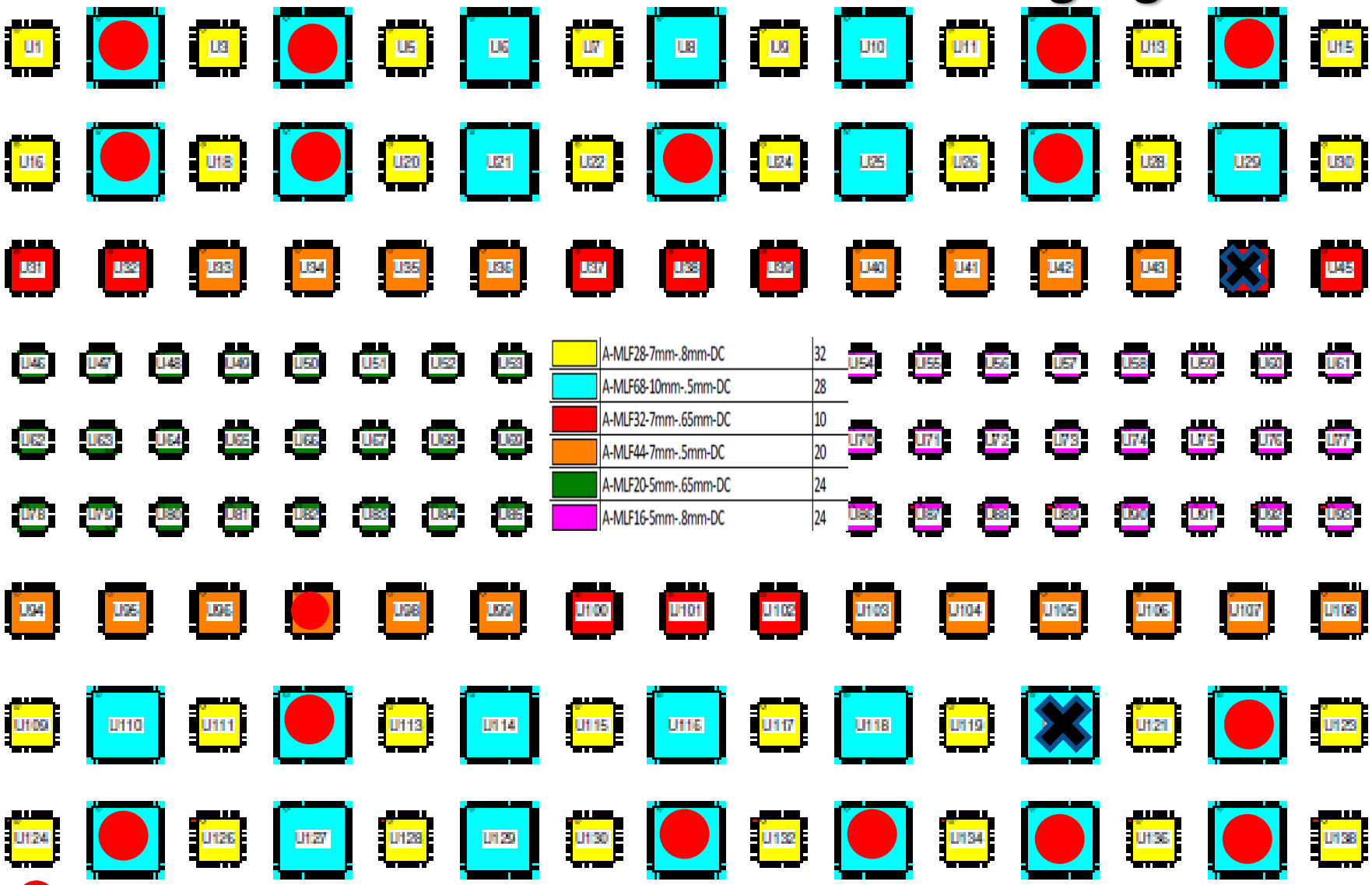

Fail Under Thermal Cycling

No Part or Fail As Received



Reza Ghaffarian/JPL/Caltech

# QFN Failure 1116 TSC2 SnPb with Pre-Aging




Fail Under Thermal Cycling

No Part or Fail As Received



Reza Ghaffarian/JPL/Caltech

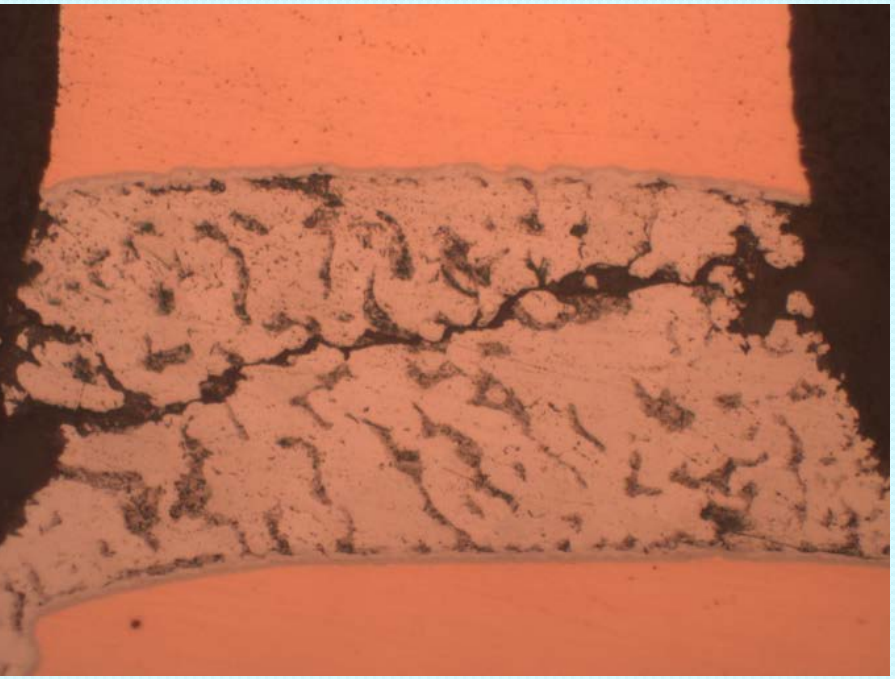
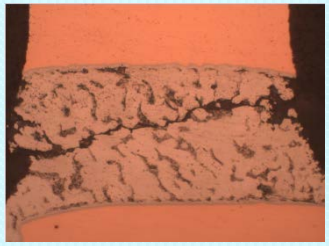
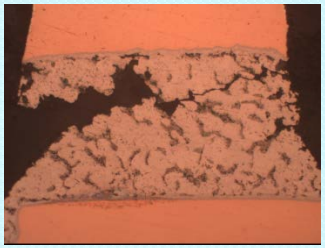
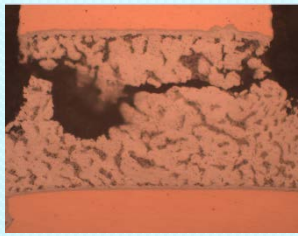
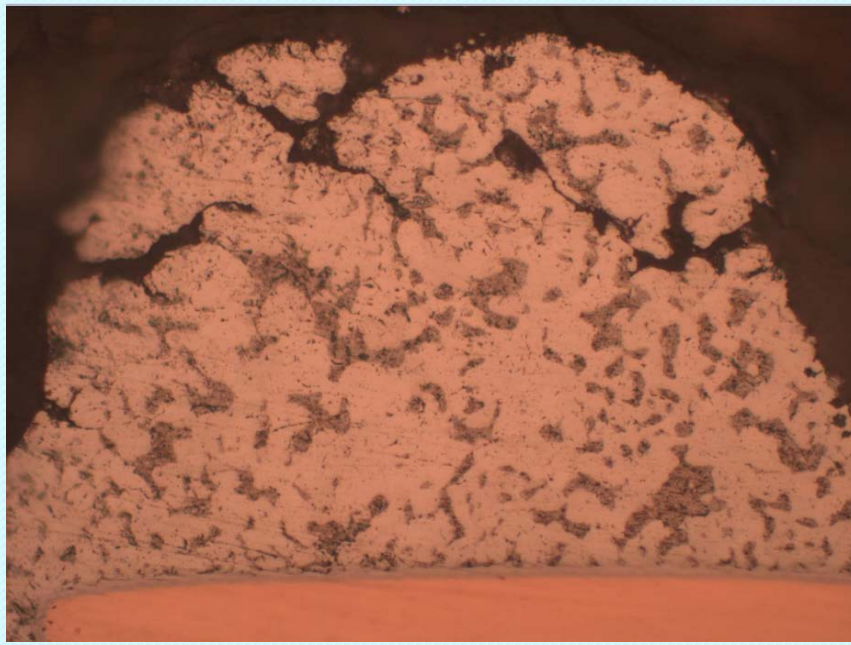
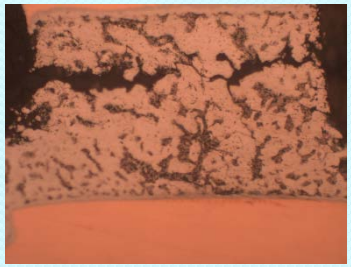
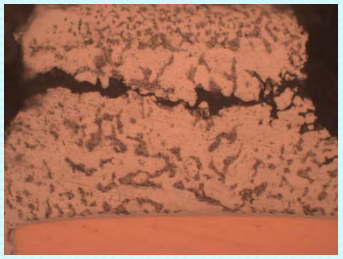
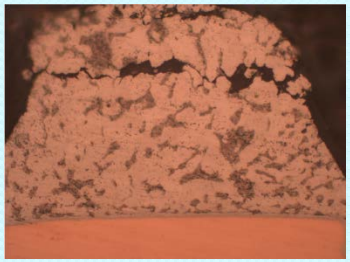
| QFNs / Cycles Only | MLF16-5-0.8 Total # of Failures | MLF28-7mm-0.8 Total # of Failures | MLF68-10-0.5 Total # of Failures |
|---|---|---|---|
| 1x186= 186 | 0 | 0 | 0 |
| 2x186= 336 | 0 | 0 | 0 |
| 3x186= 558 | 0 | 0 | 1 |
| 4x186= 744 | 0 | 1 | 1 |
| 5x186= 930 | 0 | 1 | 6 |
| 6x186=1116 | 1 | 5 | 17 |

**TSC2 Only**

**Age + TSC2**

| QFNs / Age+Cycles | MLF16-5-0.8 Total # of Failures | MLF28-7mm-0.8 Total # of Failures | MLF68-10-0.5 Total # of Failures |
|---|---|---|---|
| 1x186= 186 | 0 | 0 | 0 |
| 2x186= 336 | 0 | 0 | 0 |
| 3x186= 558 | 0 | 0 | 0 |
| 4x186= 744 | 0 | 0 | 0 |
| 5x186= 930 | 0 | 0 | 2 |
| 6x186=1116 | 0 | 0 | 13 |

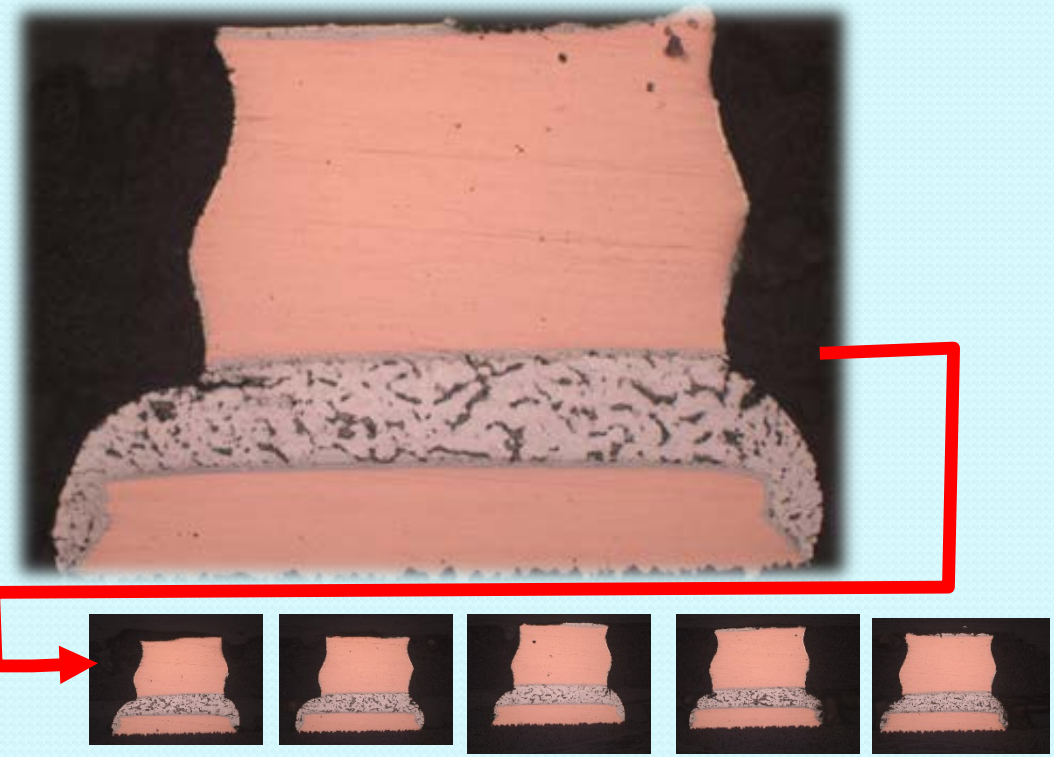
# MLF68-10mm

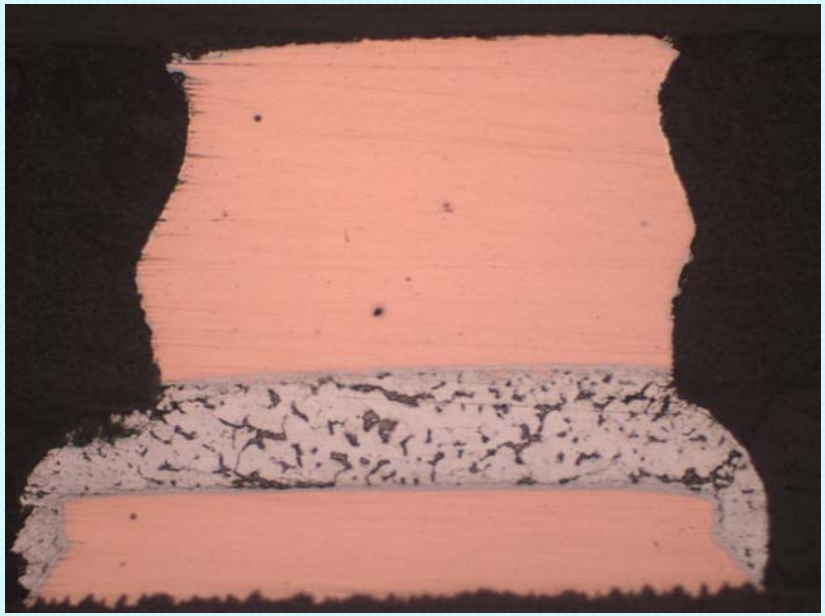











***Reza Ghaffarian/JPL/Caltech***

# MLF28-7mm

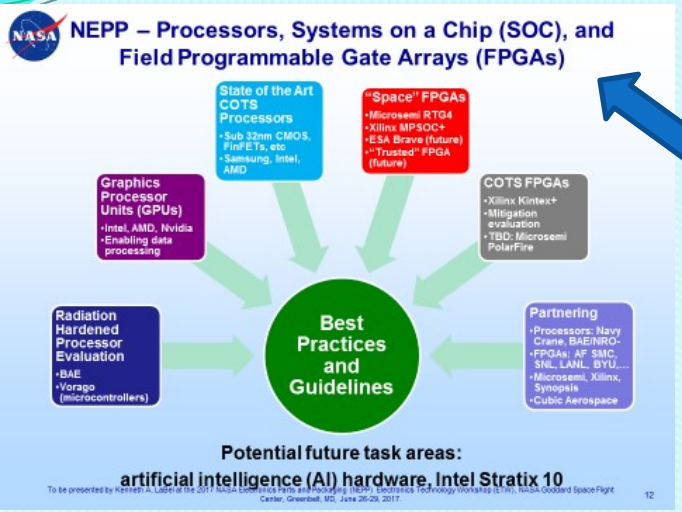




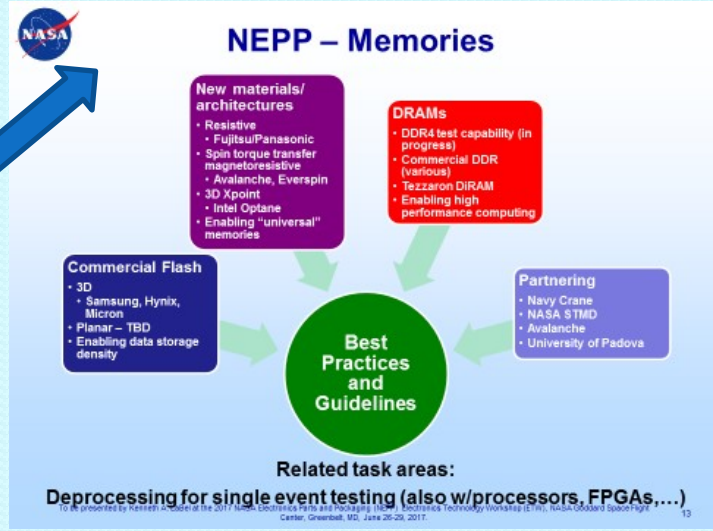
# Summary

- Released NEPP report
- No failure to 200 TC cycles (–55°/100°C)
  - Assemblies with tin-lead solder
  - Cycling stopped @ 200 ~
- A large number of failures for MLF 68 I/O
  - 1166 thermal shock cycles only (–55° to 125°C)
  - 250 hours age at 125°C & 1166 TSC cycles.
- Pre-aged had lower failures
- X-sections confirmed daisy-chain results
  - MLF68 showed full cracking
  - MLF28 showed only minor microcracking
- COTS QFNs to 68 I/Os are robust

# TMV/TSV TC Reliability

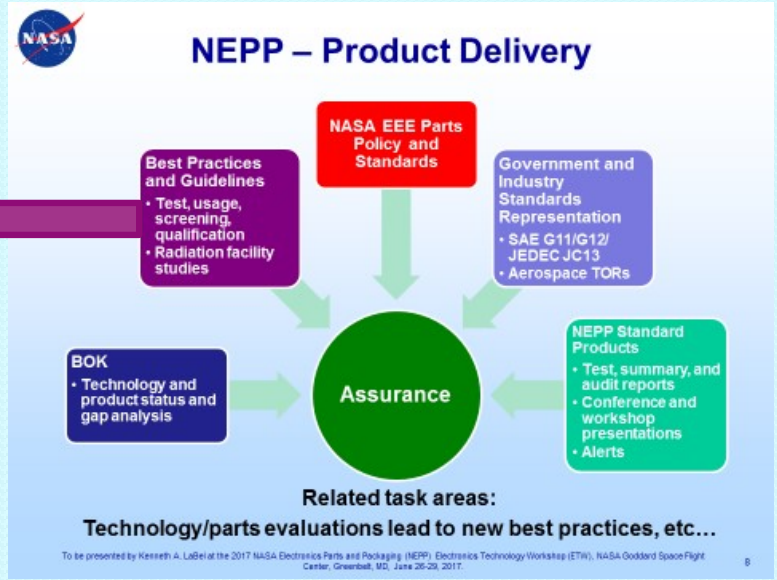



Guideline
Test Results
NEW
NEPP TASK




## Best Practices and Guidelines

- Test, usage, screening, qualification
- Radiation facility studies






*Reza Ghaffarian/JPL/Caltech*

# Electronics Roadmap

***iNEMI :***

- ITRS to IRDS (device & system)
- Re-stores Defense/Aerospace
- Data centers as utilities & clouds as “rent vs. buy”
- Assembly to lower cost/temp Pb-free
- The “IoT”, sensors ubiquitous- cyber-attacks?
- Portables shift to “wearables”
- Auto safety systems to proliferate
- Remote patient care, proactive/preventive

# Packaging as Enabler of Moore's Law Scaling

- Historically
  - Silicon growth by Moore's law
  - Packaging supporting role
  - Packaging focused on powering performance and silicon latency
- Now, Packaging is differentiator
  - Wafer level package (WLP), fan-in & fan-out
  - Embedded passive/active
  - System on package (SoP), System in package (SiP), and Heterogeneous integration (HI)
  - Complex products: SiP (2.5D & 3D)
  - Through-silicon-via (TSV) to compete with optical on chip

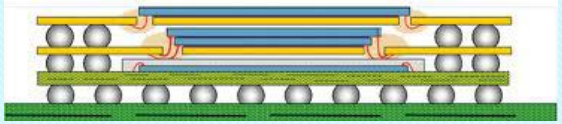
# 2.5D/3D Packaging

Stack Die
PoP

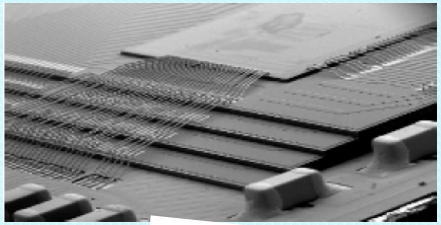
*2D to 2.5 D*
*Single Chip to Multi-chip*
*TSV for Interposer*

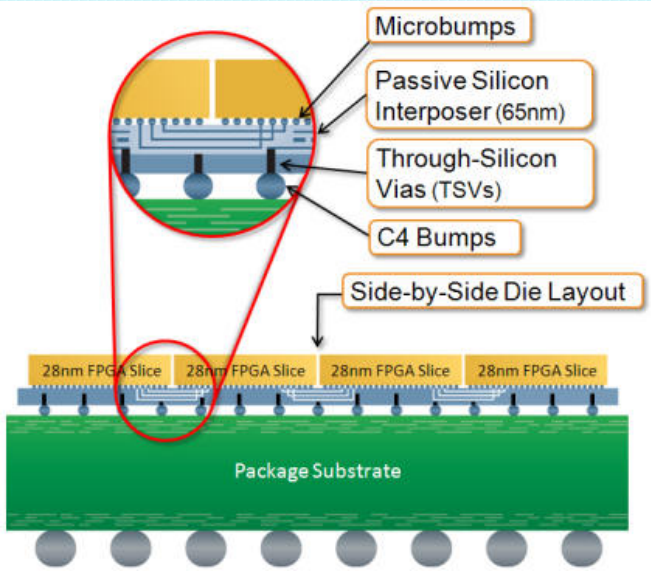
2.5D to 3DTSV
3D SIP

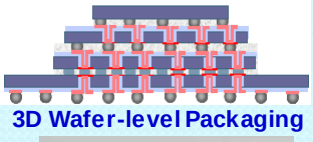
**Package on Package (PoP)**



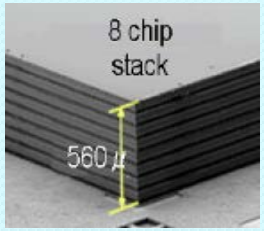
**3D Wire Bond**



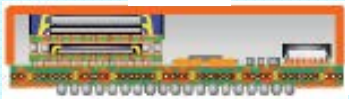



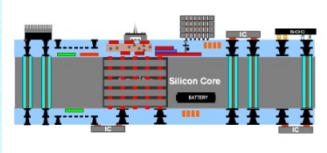
**3D Wafer-level Packaging**




**Through-silicon Via**

***3D SiP***

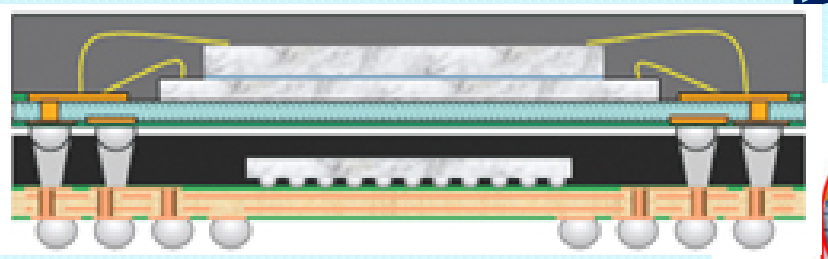




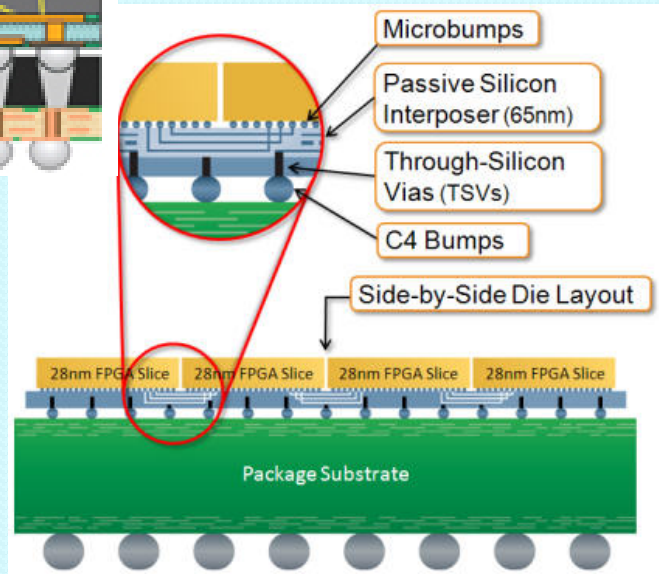
# TMV/TSV Packaging Evaluation

TMV

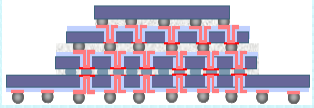
**Through Mold Via (TMV)**



*2.5 D SIP*




3D TSV



**3D Wafer-level Packaging**

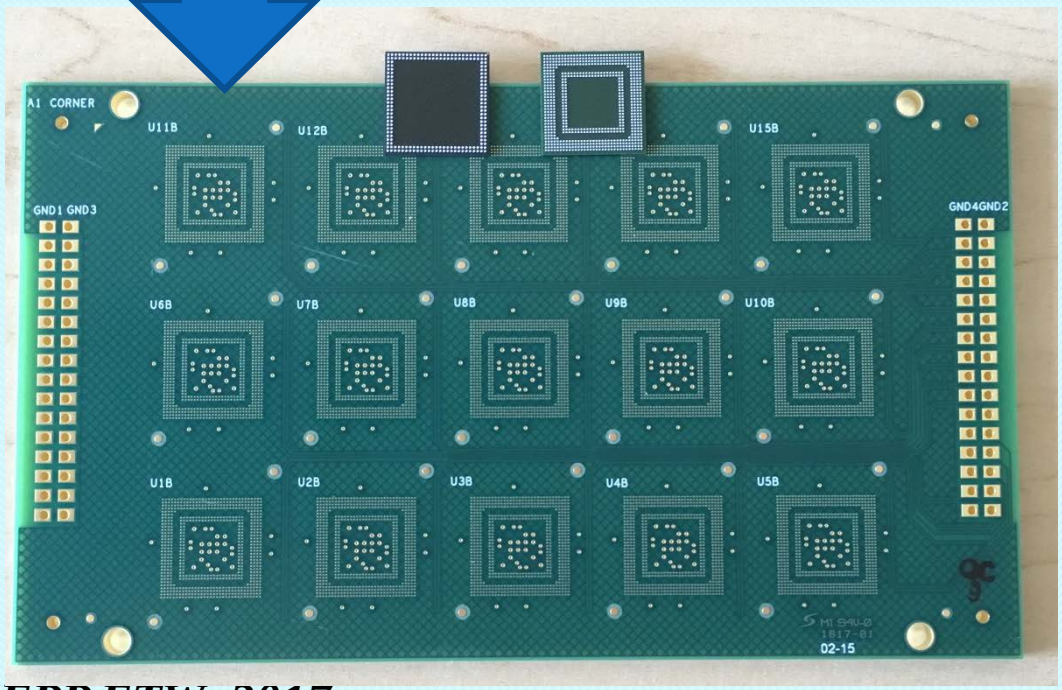
# TMV/TSV Packaging Status

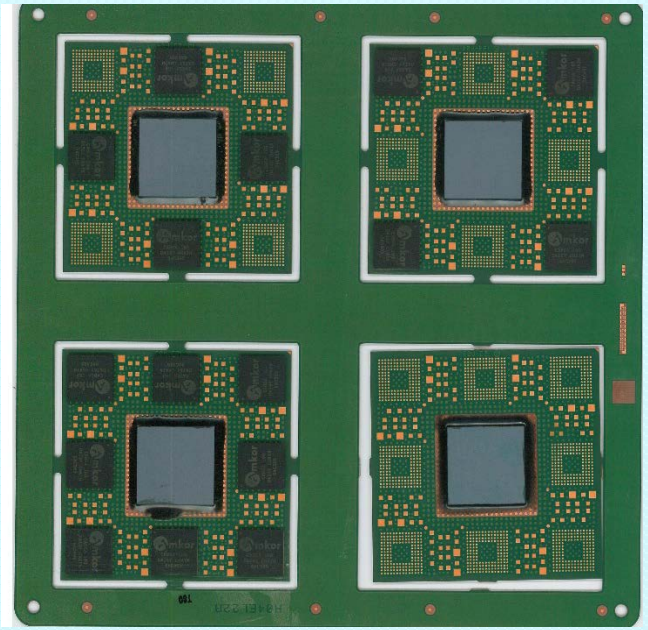
TMV

**Through Mold Via (TMV)**

***2.5 D SIP***

3D TSV



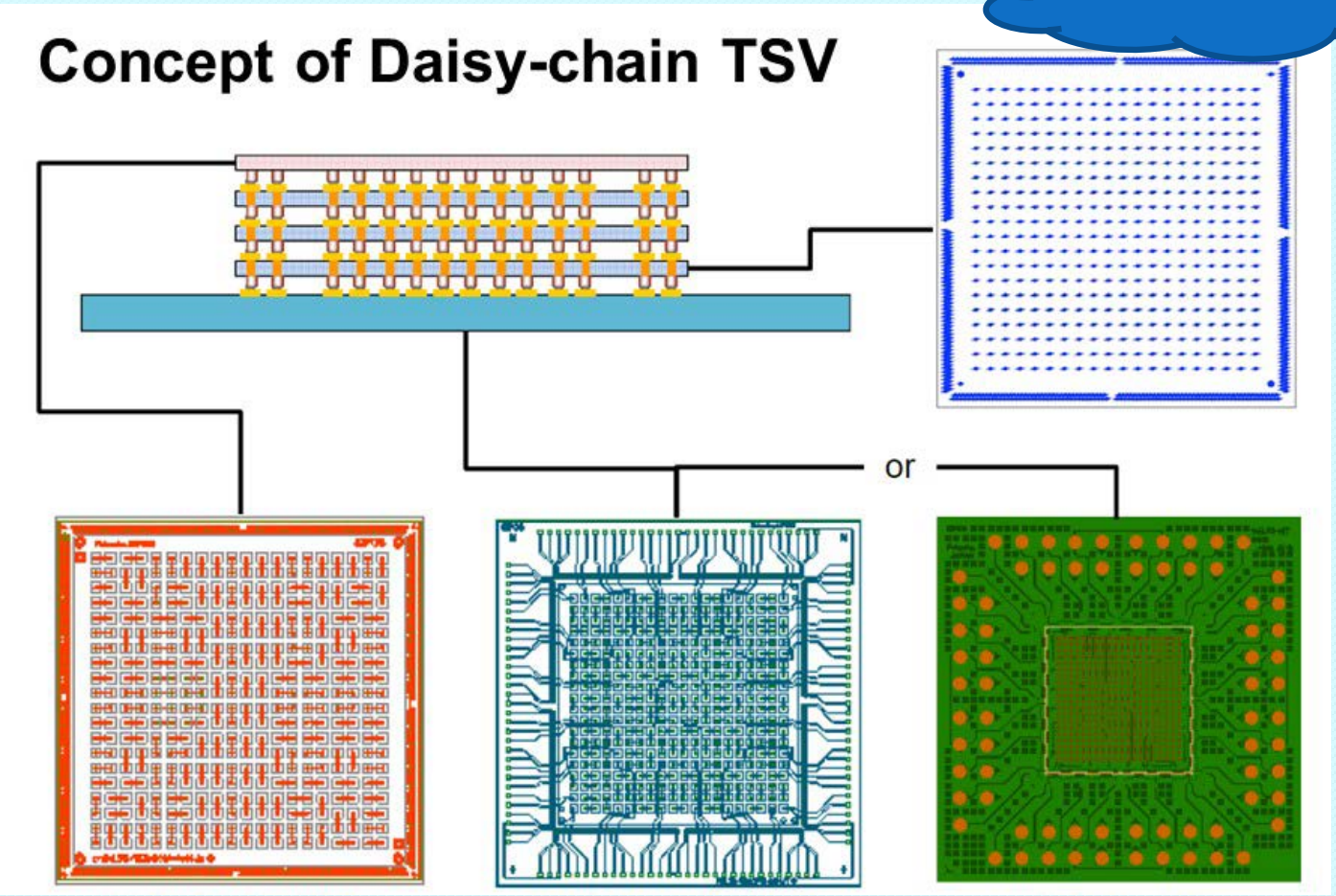





***Reza Ghaffarian/JPL/Caltech***

# TMV/TSV Packaging Status

3D TSV



# NEPP TMV/TSV

- Challenges package/2nd Level Reliability
  - Availability of COTS packages
  - Assembly challenges/Reliability testing
- Through mold via (TMV) stack
  - Packages/PCBs are ready to assemble
- 2.5D (Joint effort Univ/Industry)
  - First article built successfully
  - Additional build and Reliability
- Daisy-chain TSV
  - Concept is finalized
  - Numerous options
  - Select & evaluate assembly/reliability

# Acknowledgment

The research described in this publication is being conducted at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. Copyright 2017 California Institute of Technology. U.S. Government sponsorship acknowledged.

The author would like to acknowledge the support of the JPL team and industry partners. The author also extends his appreciation to the program managers of the National Aeronautics and Space Administration Electronics Parts and Packaging (NEPP) Program.

**http://nepp.nasa.gov**

**Thank You!**